REMARKS/ARGUMENTS

Favorable consideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1, 3, 4, 6-8, 11 and 12 are presently pending in this application, Claims 2, 5, 9, 10 and 13-17 having been canceled, Claims 1, 3, 4, 6-8, 11 and 12 having been amended by the present amendment.

In the outstanding Office Action, Claims 1, 3-6, 16-17 were rejected under 35 U.S.C. §102(b) as being anticipated by Asai et al. (U.S. Patent 6,534,723); Claims 2, 7-15 were rejected under 35 U.S.C. §102(b) as being anticipated by Londa (U.S. Patent 5,963,430).

Claims 1, 3, 4, 6-8, 11 and 12 have been amended herein. These claim amendments are believed to find support in the specification, claims and drawings as originally filed, and no new matter is believed to be added thereby. If, however, the Examiner disagrees, the Examiner is invited to telephone the undersigned who will be happy to work in a joint effort to derive mutually satisfactory claim language.

Before addressing the rejections based on the cited references, a brief review of Claim 1 as currently amended is believed to be helpful. Claim 1 is directed to a multi-layer printed wiring board and recites: "a first substrate having an opening and having a plurality of external terminals positioned to be connected to a package substrate; a second substrate laminated to the first substrate and having a plurality of external terminals positioned to be connected to a mother board, the second substrate having a metallic layer portion in the opening of the first substrate and a plurality of non-through holes filled with conductive material and connected to the metallic layer portion; and an IC component having a plurality of terminals and loaded in the opening of the first substrate such that the terminals of the IC component face an opposite side of the metallic layer portion of the second substrate."

By providing such a second substrate, heat generated by the IC component is effectively radiated to and removed through the metallic layer portion and the non-through holes connected to the metallic layer portion in the second substrate, thereby preventing heat damage caused by the IC component.

It is respectfully submitted that neither Asai et al. nor Londa teaches or suggests "a second substrate laminated to the first substrate and having a plurality of external terminals positioned to be connected to a mother board, the second substrate having a metallic layer portion in the opening of the first substrate and a plurality of non-through holes filled with conductive material and connected to the metallic layer portion" as recited in amended Claim 1. Therefore, the structure recited in Claim 2 is believed to be distinguishable from Asai et al. and Londa, and because Asai et al. and Londa fail to disclose the second substrate as recited in amended Claim 1, their teachings even in combination are not believed to render the multi-layer printed wiring board recited in Claim 1 obvious.

For the foregoing reasons, Claim 1 is believed to be allowable. Furthermore, since Claims 3, 4, 6-8, 11 and 12 depend directly or indirectly from Claim 1, substantially the same arguments set forth above also apply to these dependent claims. Hence, Claims 3, 4, 6-8, 11 and 12 are believed to be allowable as well.

In view of the amendments and discussions presented above, Applicants respectfully submit that the present application is in condition for allowance, and an early action favorable to that effect is earnestly solicited.

Respectfully submitted,

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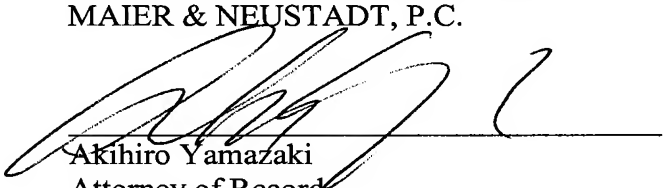

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